Neuromorphic computing architecture based on serially connected magnetic tunnel junctions

P. Rzeszut,[1] J. Chęciński,[1] I. Brzozowski,[1] S. Ziętek,[1] and W. Skowroński[1]

[1] *AGH University of Science and Technology, Institute of Electronics, Al. Mickiewicza 30, 30-059 Kraków, Poland*

Neuromorphic computing architectures have superior properties over conventional computers in solving a number of problems such as image or voice recognition, combinatioral optimization, or prediction[1]. As a concept, neural networks (NN) have been proved to be fast and flexible. However, their implementations in conventional digital architecture require large amount of resources, as subsequent multiplication and addition operations need to be performed for each input (synapse) of a single neuron.

Here, we present a complete architecture for neuromorphic computing including: multi-bit cell forming a programmable synaptic weight, electronic neuron and artificial NN together with simulation results of a representative problem solution.

The proposed multi-state cells (MSC) are realized as serially connected magnetic tunnel junctions (MTJ), where N MTJs cells create $N+1$ discrete resistance states [2], which store a synaptic weight of a neuron. A single electronic neuron is implemented as a circuit involving voltage inputs (as synapses), voltage output (which might be connected to a second layer of neurons, or act as an output), pairs of MSC, differential amplifier and a sigmoidal transient function generator. Each weight is stored as a pair of MSC at each synapse and manipulating resistance balance between these two MSC related to each input, positive, negative or zero weights may be achieved.

To verify the viability of the concept, MNIST[3] database of handwritten numbers was used as an example for NN image recognition. The network was taught using software representation on a subset of MNIST database, and the synaptic weight values were mapped to the possible memristor states. Finally, the simulations of the NN were carried out, while feeding input with different number images.

The presented design of the artificial NN might be successfully used for a wide range of applications. The proposed architecture is compliant with MRAM production technology, which has already reached 22 nm level[4], therefore, the circuits can be manufactured using the existing technology.

References:

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